



## **REMARKS**

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed February 14, 2001.

### **35 U.S.C. 102(b)(e) Rejections**

Claims 1-3 are rejected as being unpatentable over U.S. Pat. No. (hereafter ).

Specifically, the Office Action asserts that U.S. Patent No. 5,993,835 (hereafter Furukawa) teaches all limitations claimed by applicant in Claims 1-3, U.S. Patent No. 5,567,966 (hereafter Hwang) teaches all limitations claimed by applicant in Claims 4-7, and U.S. Patent No. 5,712,503 (hereafter Kim) teaches all limitations claimed by applicant in Claims 7-9.

Claim 1 as presently amended includes the limitation of the drain/source extension extending to a more shallow depth within the substrate than the drain/source terminal to which it corresponds.

Furukawa teaches several embodiments, all of which have a drain/source terminal extension that extends deeper into the substrate than the drain/source terminal to which it corresponds. Therefore, applicant has claimed a novel implementation to achieve reduced source to drain resistance while avoiding undesirable high-current effects. Therefore, that which is claimed in Claim 1 as presently amended cannot be said to be anticipated by Furukawa.

Claim 4 as presently amended includes the limitation of the drain/source extension extending to a more shallow depth within the substrate than the drain/source terminal to which it corresponds.

Hwang teaches several embodiments, all of which have a drain/source terminal extension that extends at least as deep into the substrate than the drain/source terminal to which it corresponds. Therefore, applicant has claimed a novel implementation to achieve reduced source to drain resistance while avoiding undesirable high-current effects. Therefore, that which is claimed in Claim 4 as presently amended cannot be said to be anticipated by Hwang.

Claim 7 as presently amended includes the limitation of the drain/source extension extending to a more shallow depth within the substrate than the drain/source terminal to which it corresponds.

Kim teaches several embodiments, all of which have a drain/source terminal extension that extends at least as deep into the substrate than the drain/source terminal to which it corresponds. Therefore, applicant has claimed a novel implementation to achieve reduced source to drain resistance while avoiding undesirable high-current effects. Therefore, that which is claimed in Claim 7 as presently amended cannot be said to be anticipated by Kim.

As to any remaining combinations formed by dependant claims and not specifically addressed, applicant does not concede that they are anticipated or obvious. Rather, rejections of these claims are overcome since at least the base combination is not anticipated or obvious in view of the prior art. Consequently, applicant submits that there also can be no motivation shown in the art to form the additionally limited combination claimed in such dependent claims since the prior art does not anticipate nor make obvious the base combination.

It is respectfully submitted that in view of the remarks set forth herein, the above rejections have been overcome. Accordingly, applicants respectfully submit that the claims are in condition for allowance.



**PETITION FOR EXTENSION OF TIME  
PURSUANT TO 37 C.F.R. § 1.136 (a)**

Applicant respectfully petitions pursuant to 37 CFR 1.136(a) for a three-month extension of time to file this response to the Office Action mailed February 14, 2001. The extended period is set to expire on August 14, 2001. A check in the amount of \$890.00 is enclosed to cover the fee for a three-month extension of time.

If a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Michael Bernadicou at (408) 720-8300.

Please charge any fees not covered by any checks submitted herewith to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 8/8, 2001

Michael A. Bernadicou  
Michael A. Bernadicou  
Reg. No. 35,934

12400 Wilshire Blvd.  
Seventh Floor  
Los Angeles, CA 90025  
(408) 720-8300

RECEIVED  
AUG 17 2001  
TECHNOLOGY CENTER 2800



**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**

**IN THE CLAIMS**

RECEIVED  
AUG 17 2001  
TECHNOLOGY CENTER 2800

Claims 1, 4, and 7 are amended as follows:

1. (Once Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion  
and substantially vertical sidewalls;  
a gate dielectric layer disposed superjacent the bottom portion of the recess and  
adjacent the substantially vertical sidewalls;  
a gate electrode overlying the gate dielectric layer; and source/drain terminals  
disposed in the substrate in alignment with a pair of laterally opposed gate  
electrode sidewalls;  
wherein the source/drain terminals have an extension which extends to a more  
shallow depth within the substrate than the source/drain terminals to which it  
corresponds and extends downwardly, from approximately the surface of the  
substrate, along the sidewalls of the recess.

4. (Once Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and  
tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with  
respect to the bottom portions of the recess;  
a gate dielectric layer disposed superjacent the bottom portion of the recess and  
adjacent the tapered sidewalls;

a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;  
wherein the source/drain terminals have an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess.

7. (Once Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a curvilinear shape;  
a gate dielectric layer disposed superjacent the curvilinear recess;  
a gate electrode overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;  
wherein the source/drain terminals have an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess.